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AAP INVERTER MODEL

Guidance and Performance Branch

MISSION PLANNING AND ANALYSIS DIVISION

MANNED SPACECRAFT CENTER
HOUSTON, TEXAS

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By James C. McClellan, Guidance and Performance Branch,
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FIGURE

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1.0 SUMMARY AND INTRODUCTION

In accordance with Subtask AA-30.2 Model Development of Task AA-30, EPS Support for AAP Consumables, a model has been developed to simulate the electrical performance for the AAP inverters. The mathematics of this model have been incorporated into a computer program for the electrical power system (EPS). A listing of the program, a detailed flow chart of the logic, a table of the data used in the calculations, and two sample cases which illustrate the output of the program are included in this report.

2.0 DEFINITIONS

EQUIP (9) — ac equipment list which contains the names of the ac equipment as alphanumeric information; the array dimension will have to be updated when the actual list becomes available

WATTS (9) — power of each ac equipment

PF (9) — power factor of each ac equipment

INV (6) — inverter ON/OFF status

- 0 OFF
- 1 ON

AK (6) — inverter overload capacity

HVA (2,9,3,2) — efficiency versus volt-amps data; the subscripts are as follows.

- First subscript: efficiency and volt-amps axes
  - 1 volt-amps axis (x-axis)
  - 2 efficiency axis (y-axis)
- Second subscript: number of data points
- Third subscript: three power factor dependent curves, the power factor on each curve is given by the PFC (3,2) array
- Fourth subscript: CSM/LM inverters
  - 1 CSM
  - 2 LM

PFC (3,2) — powered factor on each of the power factor dependent curves for both CSM and LM

LUMP — a flag to indicate that the input is a lump load

ITEM	ON/OFF status of the ac equipment 0 OFF 1 ON
SUMW	total watts of ac loads
SUMVAR	total vars of ac loads
VA	total volt-amps of ac loads
PFAC	power factor of total ac loads
POWF	power factor of a lump load input
EFF	efficiency
ETA(2)	array in which to store EFF for second interpolation
PI	DC power into the inverter
PQ	power lost in the inverter as heat
QDOT	Btu's per hr of heat lost
SEENA	spacecraft electrical energy network analysis

3.0 MODELING CONSIDERATIONS

An inverter may be considered as a constant power operating device. It requires a dc source of power input and, by means of the electronic circuitries, inverts this dc input into ac outputs, either single-phase or three-phase, depending on the system design requirement. A complete description of the CSM and LM/ATM inverter is given in section 4.0. As with any energy conversion devices, a certain amount of energy is lost through the conversion process, and this energy appears in the form of heat. Thus, it is essential that this generated heat be removed from the device so that a satisfactory performance will be obtained. A schematic of an inverter is presented in figure 3-1.

For the present modeling purpose, it is assumed that the heat removal scheme is adequate and that the performance of the inverter can be considered as independent of temperature.

Further, as a constant power device (i.e., $P = IE = \text{Const.}$), the voltage E considered here is the voltage across the inverter only. Any voltage differential between the inverter ground and system ground will not be included in the model.

A typical connection of a CSM inverter is shown in figure 3-2. If the SM negative bus is taken as the system ground, the voltage across the inverter is the difference between the system voltage and the voltage differential between the two ground buses.

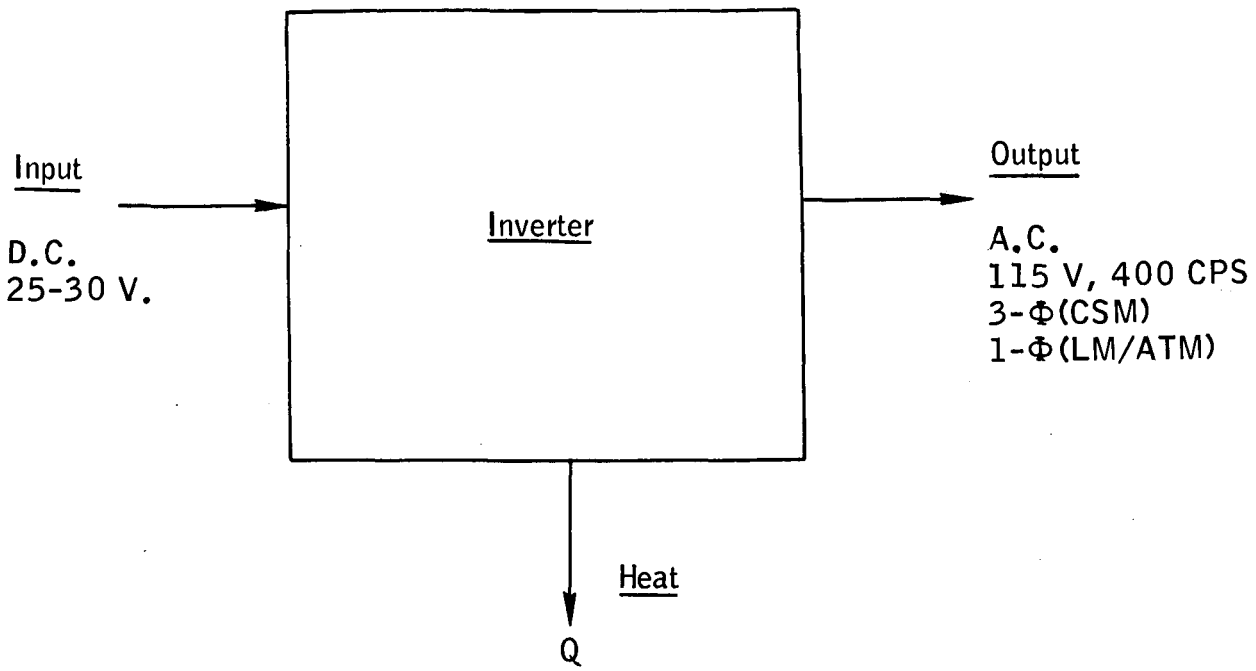


Figure 3-1.- Inverter input-output relationship.

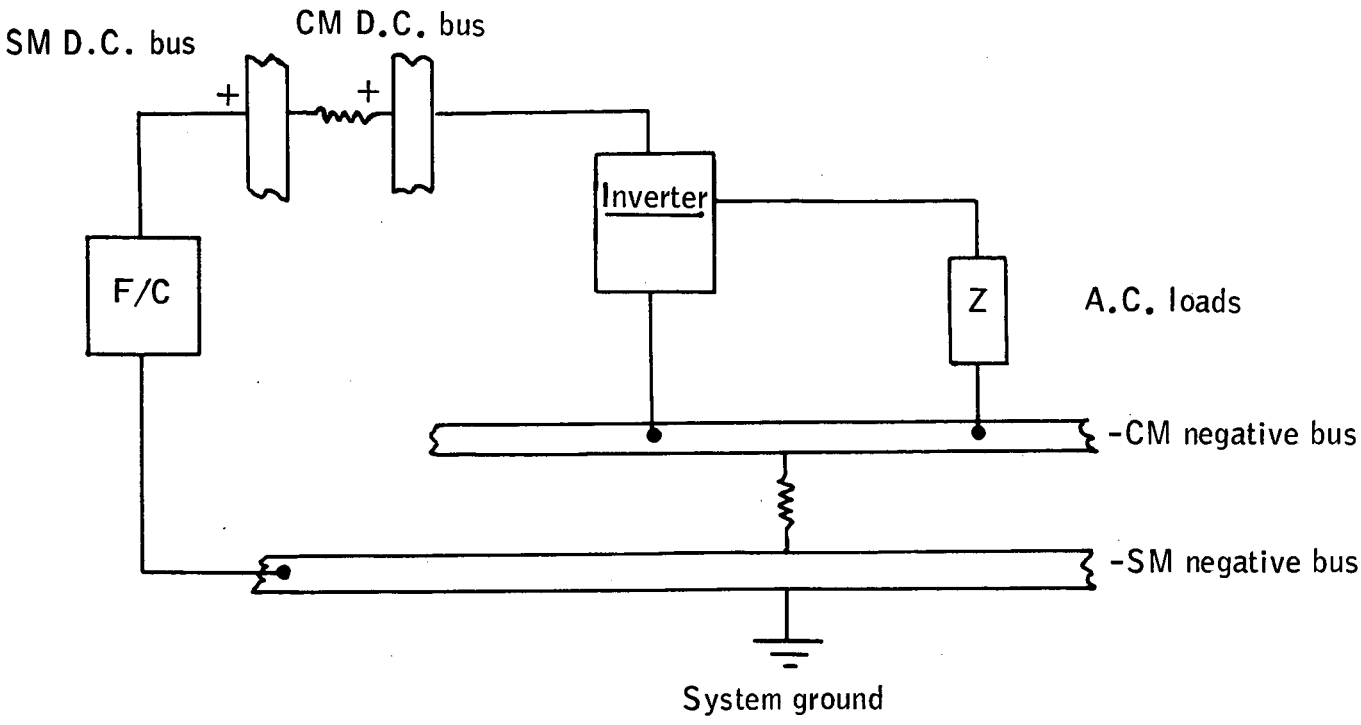


Figure 3-2.- Typical connection of inverter in the CSM distribution network.

4.0 DESCRIPTION OF INVERTERS

The inverters in the AAP electrical power system are essentially identical to those presently used in the Apollo program. At this writing, there is no information available on the AM inverters. A summary of the inverter characteristics are tabulated in table 4-1.

4.1 CSM Inverters (ref. 1)

4.1.1 Inverter description.- Each inverter (fig. 4-1) is composed of an oscillator, an eight-stage digital countdown section, a dc line filter, two silicon-controlled rectifiers, a magnetic amplifier, a buck-boost amplifier, a demodulator, two dc filters, an eight-stage power inversion section, a harmonic neutralization transformer, an ac output filter, current sensing transformers, a Zener diode reference bridge, a low-voltage control, and an overcurrent trip circuit. The inverter normally uses a 6.4-kc square wave synchronizing signal from the central timing equipment (CTE) which maintains inverter output at 400 Hz. If this external signal is completely lost, the free running oscillator within the inverter will provide pulses that will maintain inverter output within ±7 Hz. The internal oscillator is normally synchronized by the external pulse. The subsequent paragraphs describe the function of the various stages of the inverter.

The 6.4-kc square wave provided by the CTE is applied through the internal oscillator to the eight-stage digital countdown section. The oscillator has two divider circuits which provide a 1600-pp signal to the magnetic amplifier.

TABLE 4-I.- SUMMARY OF INVERTER CHARACTERISTICS

Characteristic	CSM	LM/ATM	AM
No. of inverters	3	2	No information available
Rating, ea. V-A	1250	350	
Steady-state input voltage, dc	25 to 30	24 to 32	
Steady-state output voltage, (1-n) ac	$115.5^{+1.0}_{-1.5}$	115	
Frequency, Hz	400	400	
No. of phases	3	1	
Phase rotation	A-B-C	N/A	
Power factor	.7 lag to unity	.80 lead and .65 lag to unity	
Overload, V-A	--	525	
Overload duration, min.	--	10	
Temperature	Normal and unchanged during normal operations	Normal and unchanged during normal operation	
Operation requirements	--	Inverter not operating during orbital storage period (LM-A requires no ac power during this period)	

The eight-stage digital countdown section, triggered by the 6.4-kc signal, produced eight 400-cycle square waves, each mutually displaced one pulse-time from the preceding and following wave. One pulse-time is 156 microseconds and represents 22.5 electrical degrees. The eight square waves are applied to the eight-stage power inversion section.

The eight-stage power inversion section, fed a controlled voltage from the buck-boost amplifier, amplifies the eight 400-cycle square waves produced by the eight-stage digital countdown section. The amplified square waves, still mutually displaced 22.5 electrical degrees, are next applied to the harmonic neutralization transformer.

The harmonic neutralization section consists of 31 transformer windings on one core. This section accepts the 400-cycle square-wave output of the eight-stage power inversion section and transforms in into a three-phase 400-cycle 115-volt signal. The manner in which these transformers are wound on a single core produces flux cancellation which eliminates all harmonics up to and including the fifteenth of the fundamental frequency. The 22.5° displacement of the square waves provides a means to electrically rotate the square wave excited primary windings around the three-phase, wye-connected secondary windings, which produces the three-phase 400-cycle sine wave output. This 115-volt signal is then applied to the ac output filter.

The ac output filter eliminates the remaining higher harmonics. Because the lower harmonics were eliminated by the harmonic neutral transformer, the size and weight of this output filter was reduced. Circuitry in this filter also produces a rectified signal which is applied to the Zener diode reference bridge for voltage regulation. The amplitude of this signal is a function of the amplitude of ac output voltage. After filtering, the three-phase 115-volt ac 400-cycle sine wave is applied to the ac buses through individual phase current-sensing transformers.

The current-sensing transformers produce a rectified signal, the ampliture of which is a direct function of inverter output current magnitude. This dc signal is applied to the Zener diode reference bridge to regulate inverter current output; it is also paralleled to an overcurrent trip circuit.

The Zener diode reference bridge receives a rectified dc signal, which represents voltage output, from the circuitry in the ac output filter. A variance in voltage output unbalances the bridge to provide an error signal of proper polarity and magnitude to the buck-boost amplifier through the magnetic amplifier. The buck-boost amplifier, through its bias voltage output, compensates for voltage variations. When inverter current output reaches 200 to 250 percent of rated current, the rectified signal applied to the bridge from the current sensing transformers is of sufficient magnitude to provide an error signal which causes the buck-boost

amplifier to operate in the same manner as during an overvoltage condition. The bias output of the buck-boost amplifier, controlled by the error signal, will be varied to correct for any variation in inverter voltage or an increase beyond the current output tolerance. When inverter current output reaches 250 percent of rated current, the overcurrent trip circuit is activated.

The overcurrent trip circuit monitors a rectified dc signal which represents current output. When total inverter current output exceeds 250 percent of rated current, this circuit will cause an inverter to disconnect in 15 ± 5 seconds. If current output of any single phase exceeds 300 percent of rated current, this circuit will cause an inverter to disconnect in 5 ± 1 seconds. The disconnect is provided through relays which operate in the motor switch circuits that connect the inverters to the ac buses.

The dc power to the inverter is supplied from the main dc buses through the dc line filter. The filter reduces the high frequency ripple in the input, and the 25 to 30 volts dc is applied to the silicon-controlled rectifiers.

The silicon-controlled rectifiers are alternately set by the 1600-pps signal from the magnetic amplifier to produce a dc square wave with an ON-time of greater than 90° from each rectifier. This wave is filtered and supplied to the buck-boost amplifier where it is coupled by the transformer with the amplified 1600-pps output of the magnetic amplifier to develop a filtered 35 volts dc. The filtered voltage is used for amplification in the power inversion stages.

The buck-boost amplifier also provides a variable bias voltage to the eight-stage power inversion section. The amplitude of this bias voltage is controlled by the amplitude and polarity of the feedback signal from the Zener diode reference bridge which is referenced to output voltage and current. The bias signal is varied by the error signal to regulate inverter voltage and to maintain current output within tolerance.

The demodulator circuit compensates for any low-frequency ripple (10 Hz to 1000 Hz) in the dc input to the inverter. The high-frequency ripple is attenuated by the input filters. The demodulator senses the 35-volt dc output of the buck-boost amplifier and the current input to the buck-boost amplifier. An input dc voltage decrease or increase will be reflected in a decrease or increase in the 35-volt dc output of the buck-boost amplifier, as well as a decrease or increase in current input to the buck-boost amplifier. A sensed decrease in the buck-boost amplifier voltage output is compensated for by a demodulator output, coupled through the magnetic amplifier to the silicon-controlled rectifiers. The demodulator output caused the silicon-controlled

rectifier switch (SCRS) to conduct for a longer time, which increases their filtered dc output. A sensed increase in buck-boost amplifier voltage output, caused by an increase in dc input to the inverter, is compensated for by a demodulator output coupled through the magnetic amplifier to the silicon-controlled rectifiers. The compensation permits the amplifiers to conduct for shorter periods, which produces a lower filtered dc output to the buck-boost amplifier. In this manner, the 35-volt dc input to the power inversion section is maintained at a relatively constant level irrespective of the fluctuations in dc input voltage to the inverter.

The low-voltage control circuit samples the input voltage to the inverter and can terminate inverter operation. Because the buck-boost amplifier provides a boost action during a decrease in input voltage to the inverter, the high boost required during a low-voltage input would tend to overheat the solid state buck-boost amplifier in an attempt to maintain a constant 35 volts dc to the power inversion section and a regulated 115-volt inverter output. As a precautionary measure, the low-voltage control will terminate inverter operation by disconnecting operating voltage to the magnetic amplifier and to the first power inversion stage when input voltage decreases to between 16 and 19 volts dc.

A temperature sensor with a range of +32° to +248° F is installed in each inverter and provides an input to the caution and warning switch (C&WS) which will illuminate a light at an inverter temperature of 241° F.

The inverter efficiency is compared with load in volt-amperes for power factors of 0.7, 0.9 lag and 1.0 in figures 4-2, 4-3, and 4-4, respectively. Input dc voltages of 25, 28, and 30 are given in each figure.

4.1.2 Inverter operation and application.- Distribution of ac power is accomplished with a four-wire system through two redundant buses, ac bus 1 and ac bus 2. The ac neutral bus is connected to the single-point ground. The ac power is provided by one or two of the solid-state 115/200-volt 400-Hz three-phase inverters. The dc power is routed to the inverters through the main dc buses. Inverter 1 is powered through dc main bus A; inverter 2, through dc main bus B; and inverter 3, through either dc main bus A or B by switch selection. Each of these circuits has a separate circuit breaker and a power control motor switch. All three inverters are identical and are provided with over-temperature circuitry. A light indicator illuminates to indicate an overtemperature situation. Inverter output is routed through a series of control motor switches to the ac buses. Six switches control motor switches which operate contacts to connect or disconnect the inverters from the ac buses. The motor switch circuits are designed to prevent

the connection of two inverters to the same ac bus at the same time. The ac loads receive power from either ac bus through bus selector switches. In some instances, a single phase is used for operation of equipment; and in others, all three phases are used. Over-and undervoltage and overload sensing circuits are provided for each bus. An automatic inverter disconnect is used during an overvoltage or overload. The ac bus voltage fail and overload lights in the caution/warning group provide a visual indication of voltage or overload malfunctions. The voltage of each phase on each bus is monitored by selections with the AC INDICATORS switch. Readings are displayed on the AC VOLTS meter.

4.2 LM/ATM Inverters (ref. 2)

4.2.1 Inverter description.- Two redundant 400-Hz inverters individually supply the primary ac power required in the LM. Inverter output is controlled by application of 28 volts dc from the commander's or LM pilot's 28-volt dc bus through the EPS: INV 1 and INV 2 circuit breakers, the INVERTER switch, and the AC BUS A and AC BUS B with BUS TIE circuit breakers.

The inverters are identical; therefore, only the inverter 1 circuitry is discussed. The 28 volts dc is applied through an electromagnetic interference (EMI) filter and an input filter to a dc-to-dc converter. The regulated output of the converter is changed to a 400-Hz square wave in the inverter stage. The output of the inverter stage is controlled by a 400-Hz pulse driver developed from a 6.4-kilopulse-per-second (kpps) oscillator, which is synchronized by timing pulses from the PCM. The output of the inverter stage is 400 ± 0.4 Hz, synchronized; 400 ± 10 Hz, with a free-running oscillator. The 6.4-kpps oscillator output is divided precisely by 16 in the divider logic circuit and is routed to the inverter stage, the electronic tap changer, and the short-circuit protection circuits.

The electronic tap changer sequentially selects the output of the tapped transformer in the inverter stage, which converts the 400-Hz square wave to an approximate sine wave of the same freuqency. The output filter minimizes harmonic distortion. The voltage regulator maintains the inverter output at 117 volts ac ±1 percent during normal load conditions by controlling the amplitude of the dc-to-dc converter output. The voltage regulator also compensates for variations in the dc input and ac output load. A block diagram of the inverter is shown in figure 4-5. Typical inverter efficiency curves are shown in figures 4-6 and 4-7 for dc input voltages of 24 and 32 volts, respectively. Power factors of 0.65 lag, 0.8 lead and unity are given in each figure.

4.2.2 Inverter operation and application.- The ac power is provided to LM subsystems by either of two identical, redundant inverters; it is controlled by the EPS: INV 1 and INV 2 circuit breakers, the INVERTER switch, and the AC BUS controlled by AC TIE circuit breakers on panel 11. The EPS INV 1 or INV 2 circuit breakers supply 28 volts dc from the LM pilot's or commander's 28-volt dc bus to the chosen normally synced inverter, where the dc is changed to 117-volt, 400-Hz, ac power (350 volt-amperes). The INVERTER switch selects and routes the output of either inverter to the ac buses by way of the respective AC BUS A: BUS TIE or AC BUS B: BUS TIE circuit breakers.

Normally, inverter 2 is energized when the LM subsystems are first activated and connected to the ac buses. Inverter 1 functions as a backup during the mission, except that it is the operating inverter during DPS engine burn. An ac bus voltage and frequency signal is supplied from ac bus A by the AC BUS VOLT circuit breaker to the instrumentation subsystem (IS) for telemetry and caution light display. An out-of-tolerance frequency (less than 398 Hz or more than 402 Hz) or low-voltage condition (below 112 volts ac) caused the INVERTER caution light and MASTER ALARM pushbutton/lights to go on and a tone to be generated. The crewman makes a determination of the indication and performs corrective action. The INVERTER caution light turns off when the malfunctioning condition is remedied. The MASTER ALARM light turns off and the audio tone is discontinued when the pushbutton for the MASTER ALARM light is pressed. When positioned to AC BUS, the POWER/TEMP MON selector switch selects ac bus A for voltage display on the VOLTS indicator.

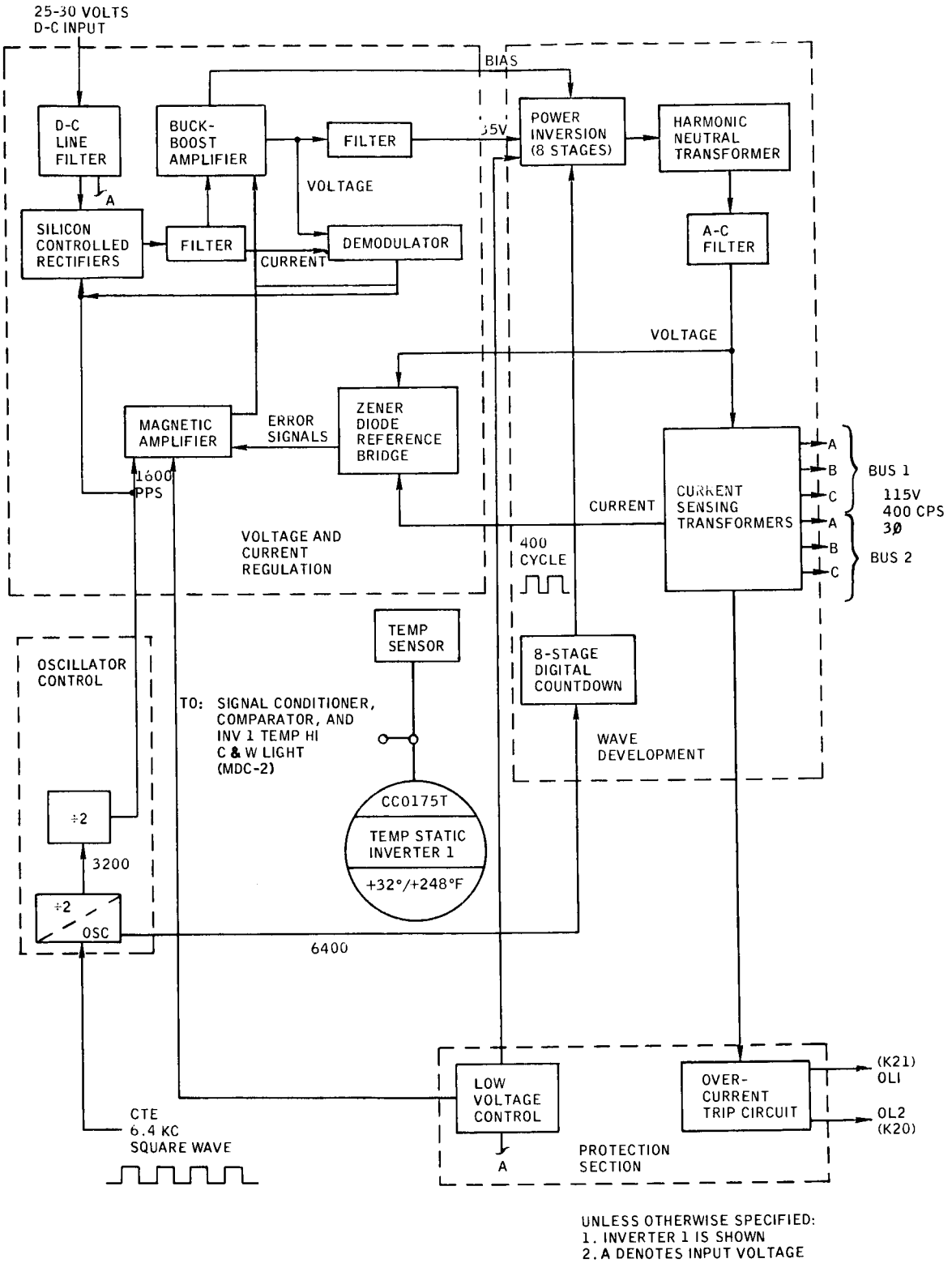


Figure 4-1.- CSM inverter block diagram.

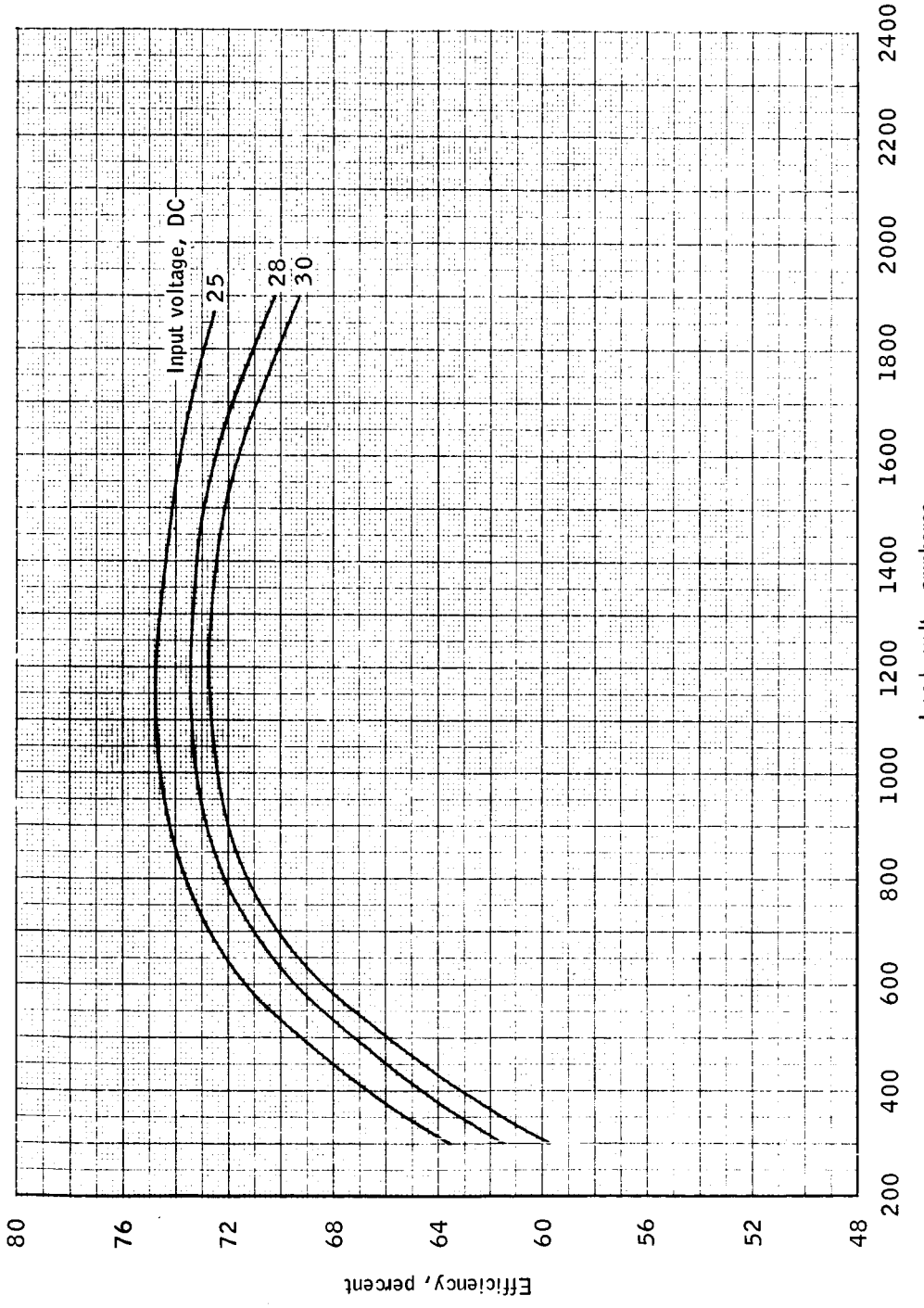


Figure 4-2.- Apollo static inverter efficiency - power factor = 0.7 lagging.

Figure 4-3. - Apollo static inverter efficiency - power factor = 0.9 lagging.

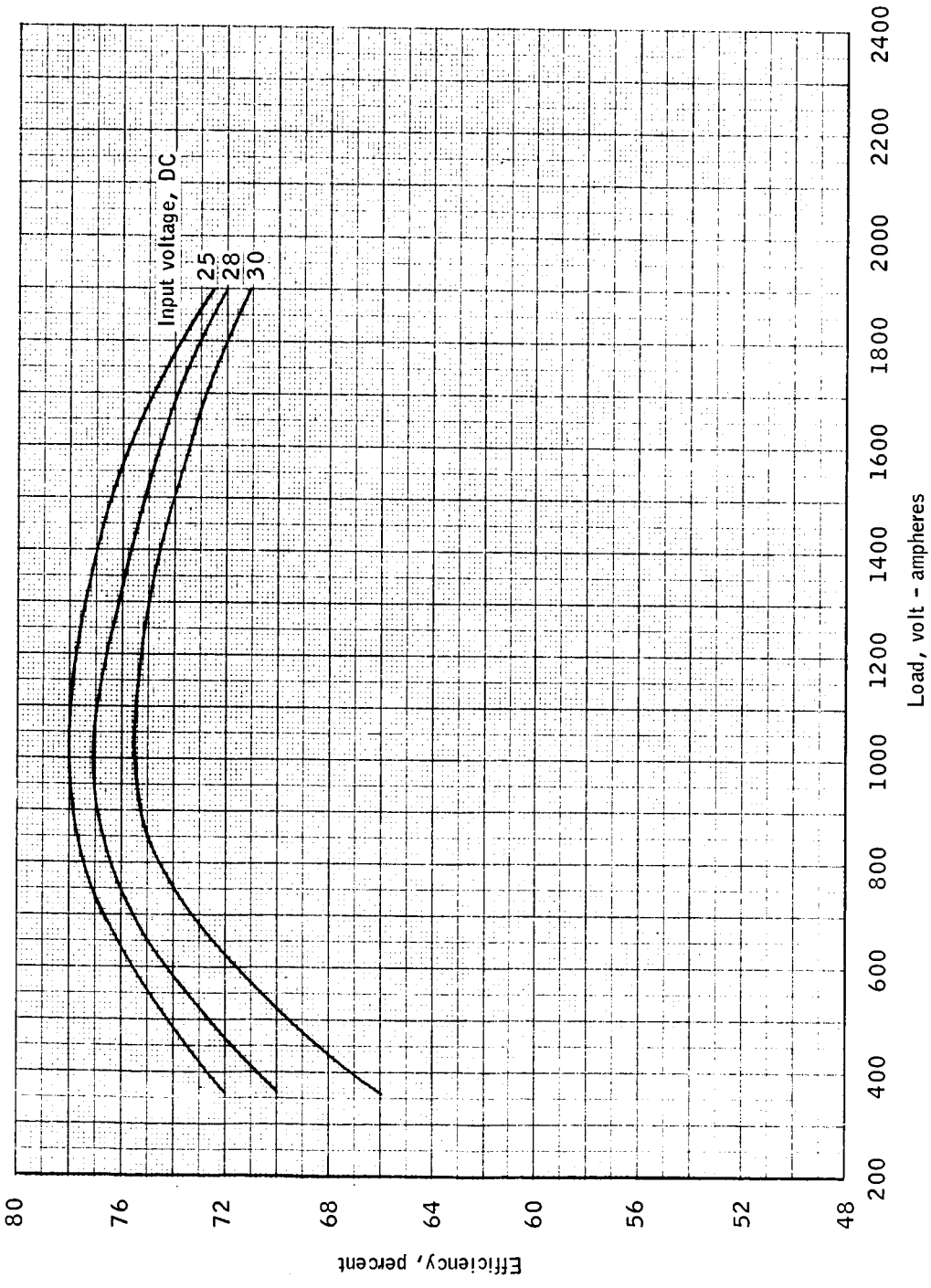


Figure 4-4.- Apollo static inverter efficiency - power factor = 1.0 unity.

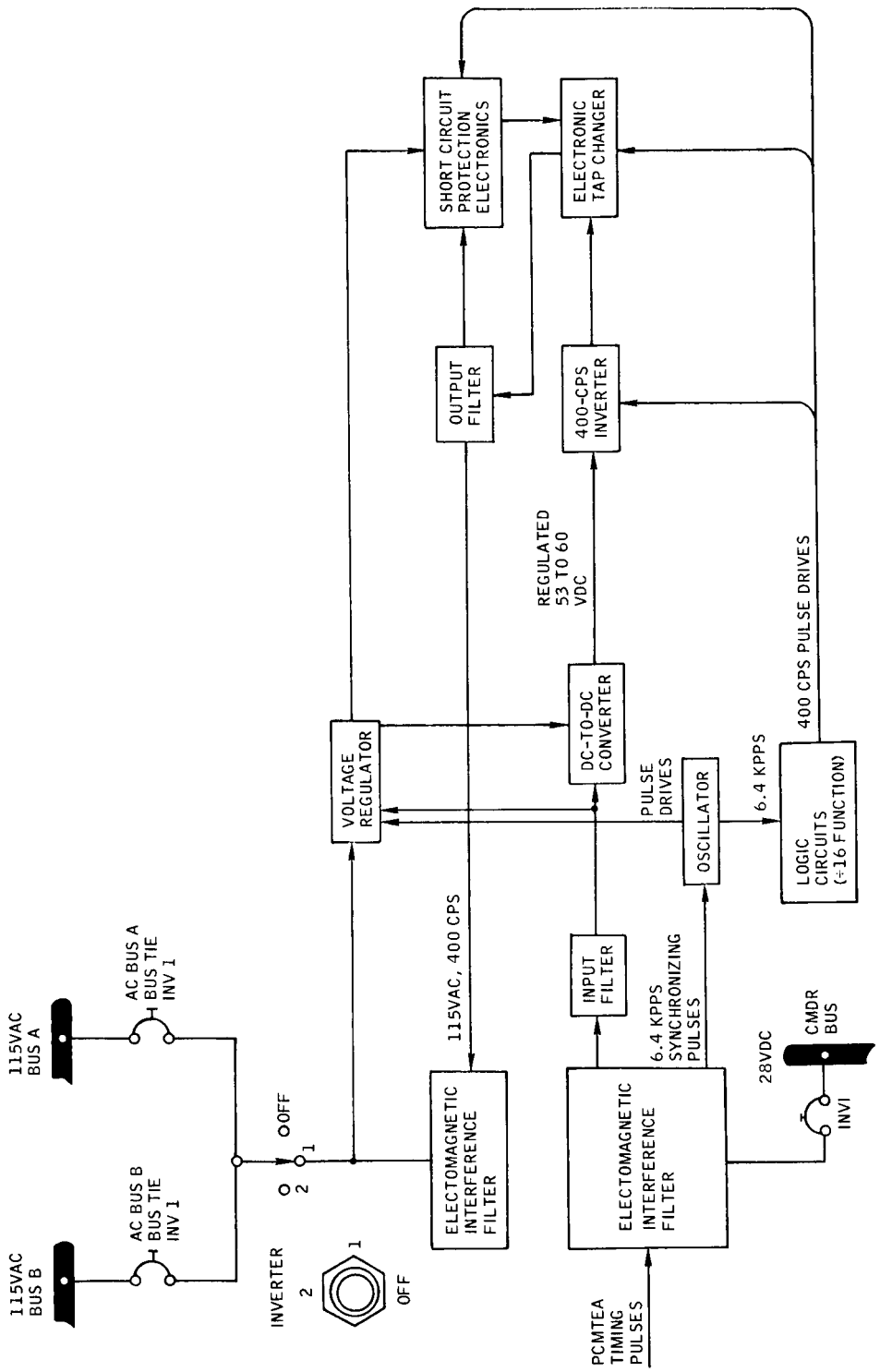


Figure 4-5.- Inverter block diagram-LM.

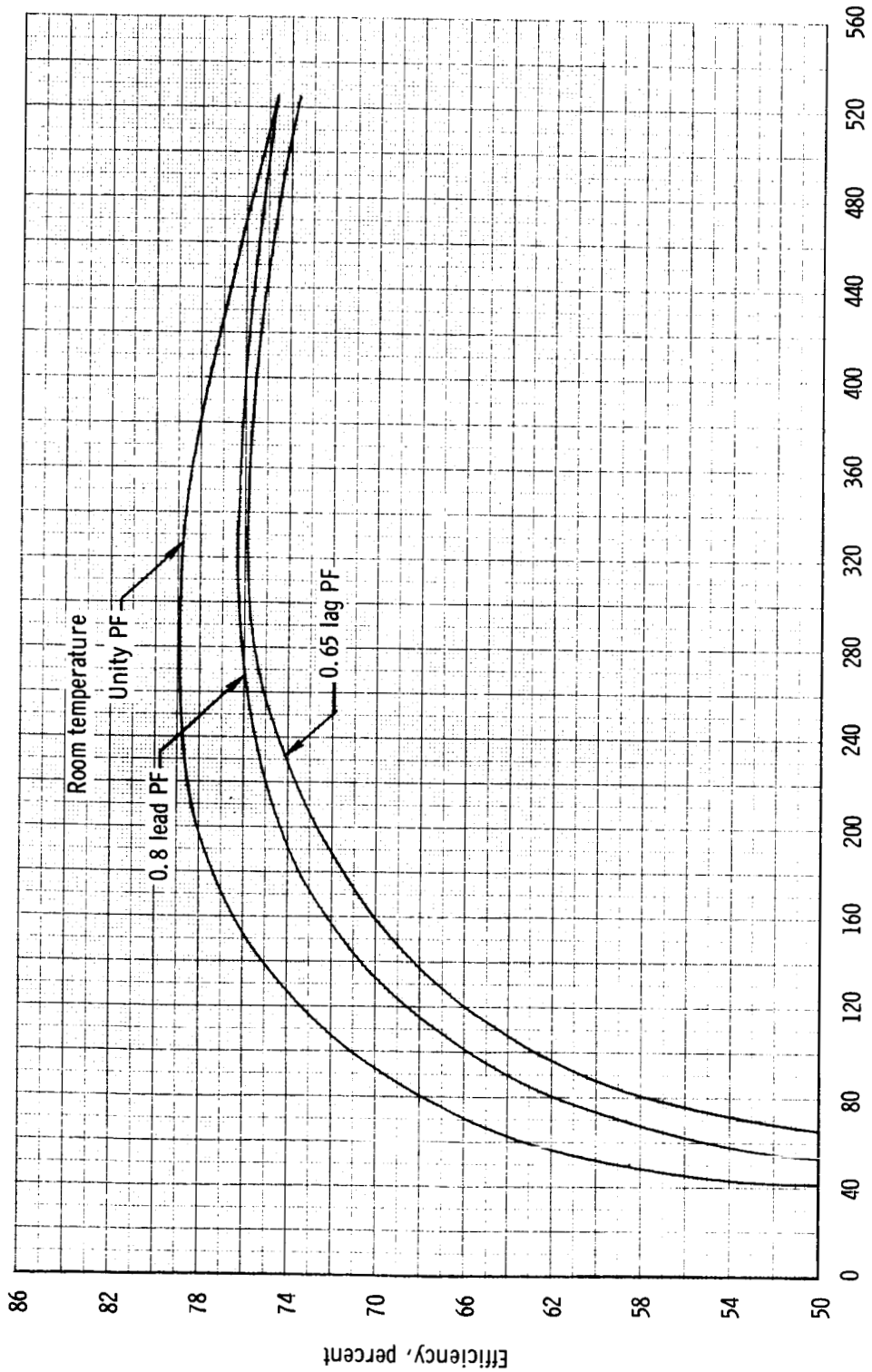


Figure 4-6. - Typical inverter efficiency, 24 VDC input voltage.

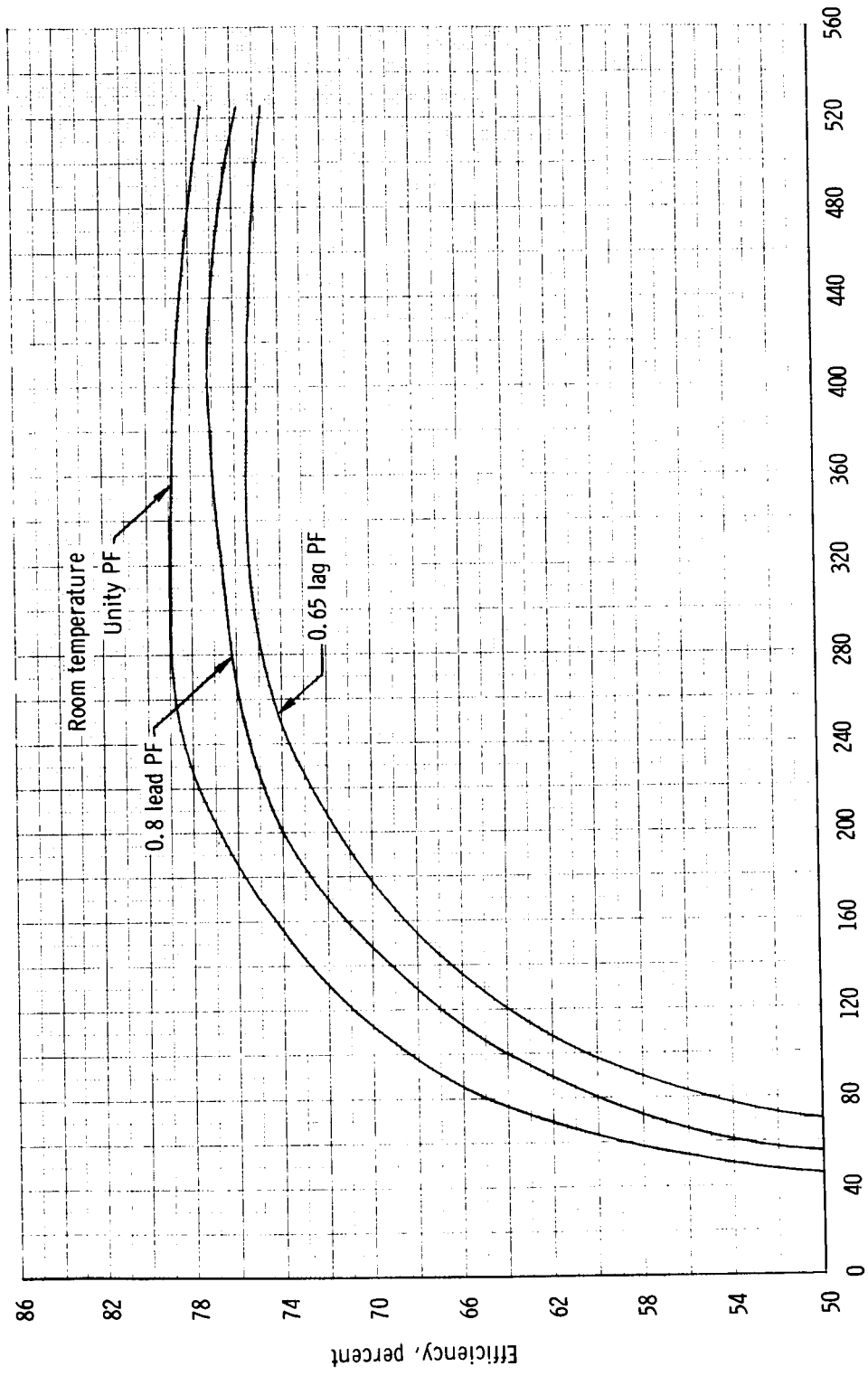


Figure 4-7.- Typical inverter efficiency, 32 VDC input voltage.

5.0 DESCRIPTION OF THE MODEL

Prior to a detailed explanation of the program logic, it is necessary to restate certain assumptions which were applied to the math model and which are used in the computer model. These assumptions are as follows.

a. There are no data available on airlock module (AM) inverters to be used in the AAP. However, the computer model will have to be altered in only a few places. These changes include updates to the dimension statements and provide the logic to follow FORTRAN statement 20 to lead into FORTRAN statement 13, where the efficiency is calculated. This logic will be similar to the logic used from FORTRAN statements 17 to 13.

b. There is no ac equipment list available at this time and also no time line with ac loads dependent on time. When this information becomes available, it can easily be incorporated into the inputs of the program. However, it is necessary that all ac equipment be rated at a common voltage.

c. All efficiency calculations are performed at 28 volts from CSM and LM curves found in the Spacecraft Operational Data Book (SODB). It is assumed that the error in calculations of the efficiency is small (less than 3 percent) over the operating range of voltages on the inverter. The data used for these calculations are presented in table 5-I.

d. When the load on the LM inverters is less than 80 volt-amps, the power lost is set to 40 watts. Data for this assumption were presented in the SODB, volume II, figure 4.3-4 in the ECS section for heat generated versus ac power.

e. The output of the program is a voltage-current (V-I) curve of constant power. With these data, the current drawn by the ac loads through the inverter can be calculated directly for any given dc bus voltage. This calculation is different from the present SEENA program which converges the solution for bus voltage and current through iterative calculations.

The program flow can be divided into three main sections.

a. Determination of the ac load on an inverter

b. Calculation of the efficiency and the input power

c. Calculation of output V-I curve

The program first searches the ac equipment list to determine which loads are on and then adds up the total watts, volt-amps, vars, and power factor

of the entire load. There is an option to enter a lumped load as input and to assign it to a particular inverter. The format for a lumped load input is to have an input data card with a 1 in column 1 as indicated by FORTRAN format statement 1, followed by a card with the watts, power factor, and inverter to which the load is to be assigned. The names of all the equipment that is on are stored in the ACLOAD array so that they can be printed out in the event of an overloaded inverter. Pages 6-1 and 6-2 of the flow chart correspond to this section.

Section b is concerned primarily with determination of the proper indices so that the correct curves can be selected for the efficiency calculation. Two interpolations are required to calculate the efficiency, one along the data curves and one between the data curves. The efficiency calculation is illustrated on pages 6-3 and 6-4 of the flow chart.

Finally, the output V-I curve is calculated from the input power, which is the output power divided by the efficiency. Twenty-six data points from 10 to 35 are calculated and stored in the arrays volt (26) and AMP (26). Also, the power lost, which is the difference between the power out and the power in, is assumed to be converted to heat. The conversion factor of 3.412 is used to convert the power lost from watts to Btu's/hr. The logic of section c is shown on page 6-5 of the flow chart.

The V-I curve and the heat are available as outputs and can be used in the EPS and ECS programs, respectively. Plots of the V-I curve of constant power for the two test cases which were run are presented in figures 8-1 and 8-2.

TABLE 5-I.- DATA (EFF vs. VA)

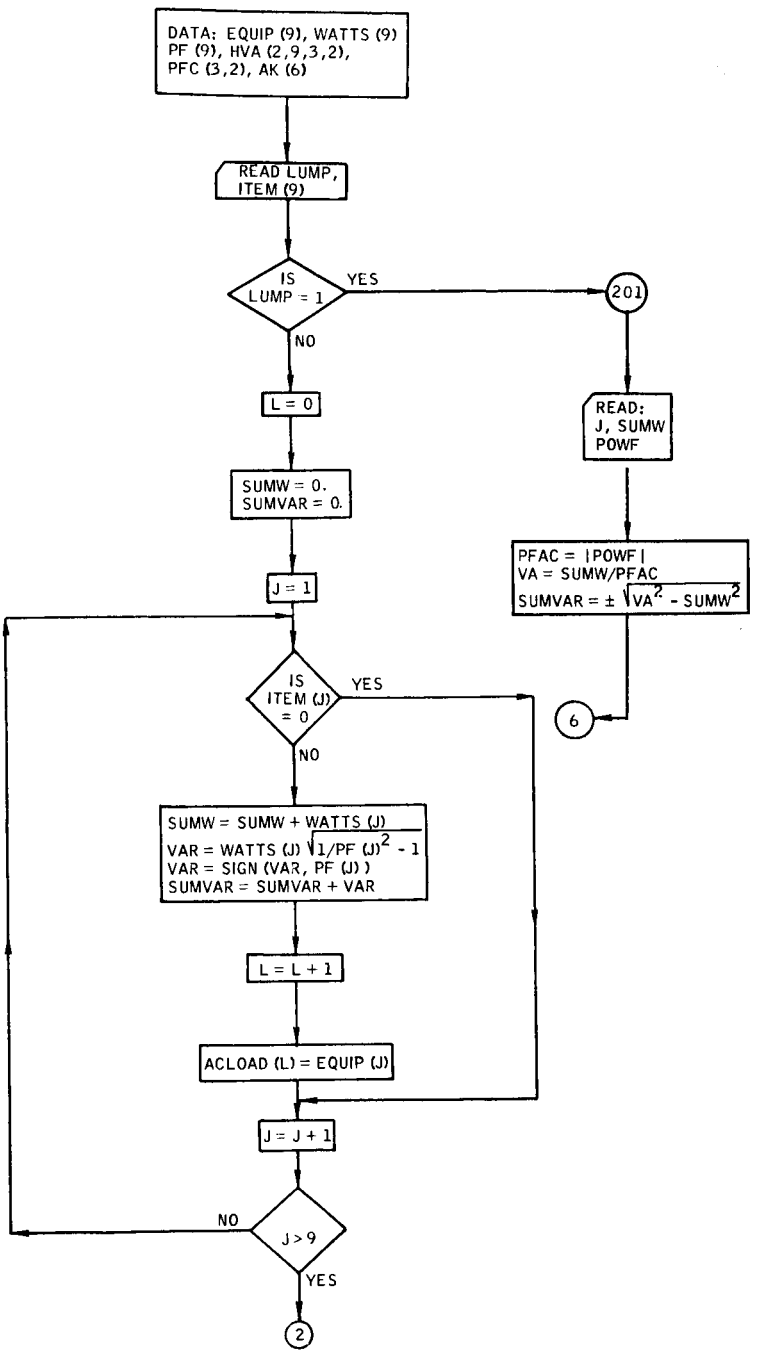
(a) CSM

0.7 lag		0.9 lag		1.0	
VA	EFF	VA	EFF	VA	EFF
300	0.615	300	0.662	350	0.7
460	.666	470	.712	520	.73
625	.698	690	.746	700	.756
795	.721	900	.762	800	.767
1000	.732	1070	.764	910	.77
1200	.736	1290	.76	1160	.768
1400	.734	1500	.754	1500	.75
1600	.726	1635	.747	1630	.743
1900	.702	1810	.73	1900	.72

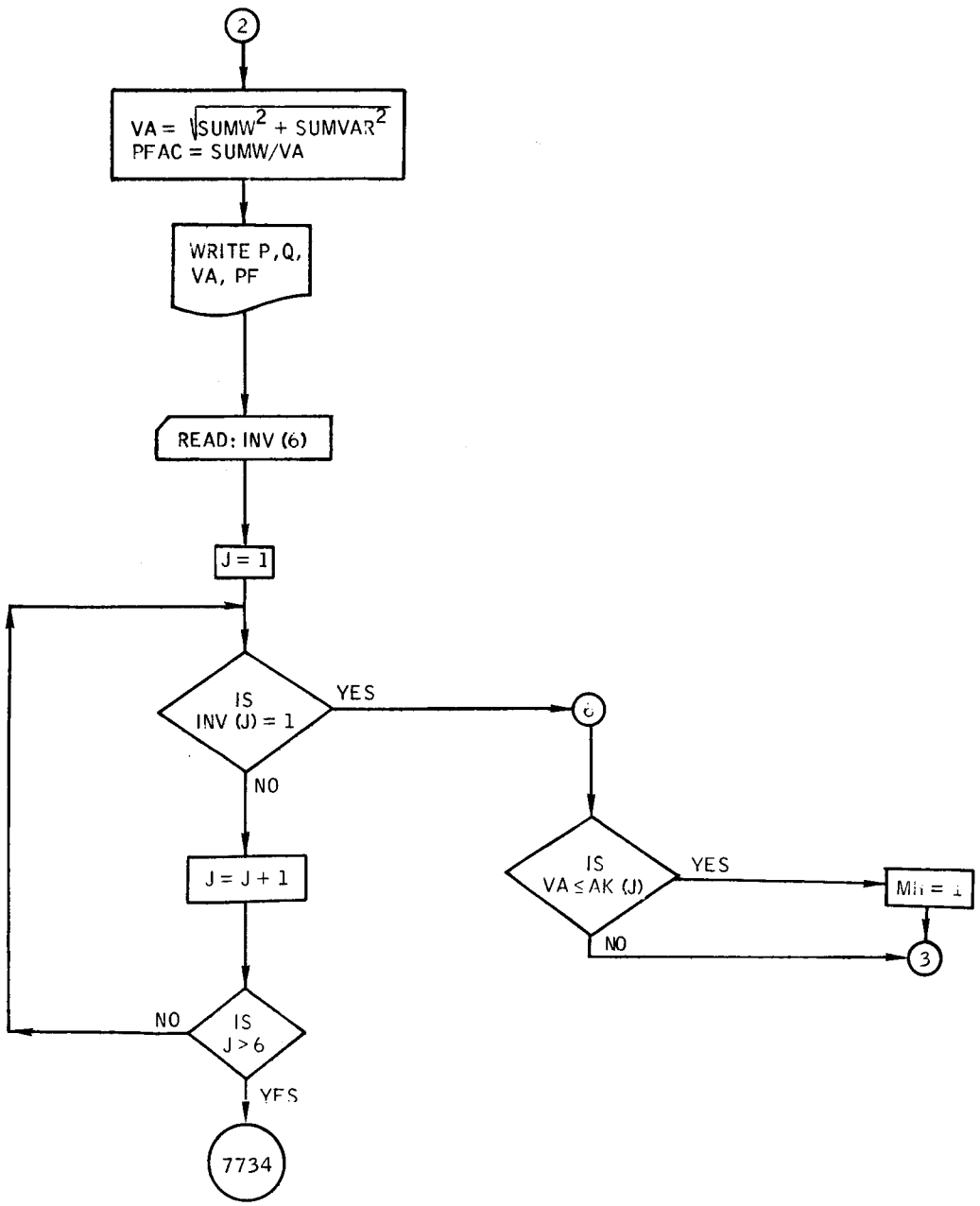
(b) LM

0.65 lag		1.0		0.8 lead	
VA	EFF	VA	EFF	VA	EFF
68	0.5	75	0.652	75	0.6
81	.575	108	.71	90	.635
112	.642	140	.742	125	.688
160	.697	185	.772	175	.728
218	.733	240	.785	225	.748
280	.754	280	.79	290	.76
345	.758	368	.786	360	.768
425	.754	430	.781	428	.765
500	.743	500	.768	500	.755

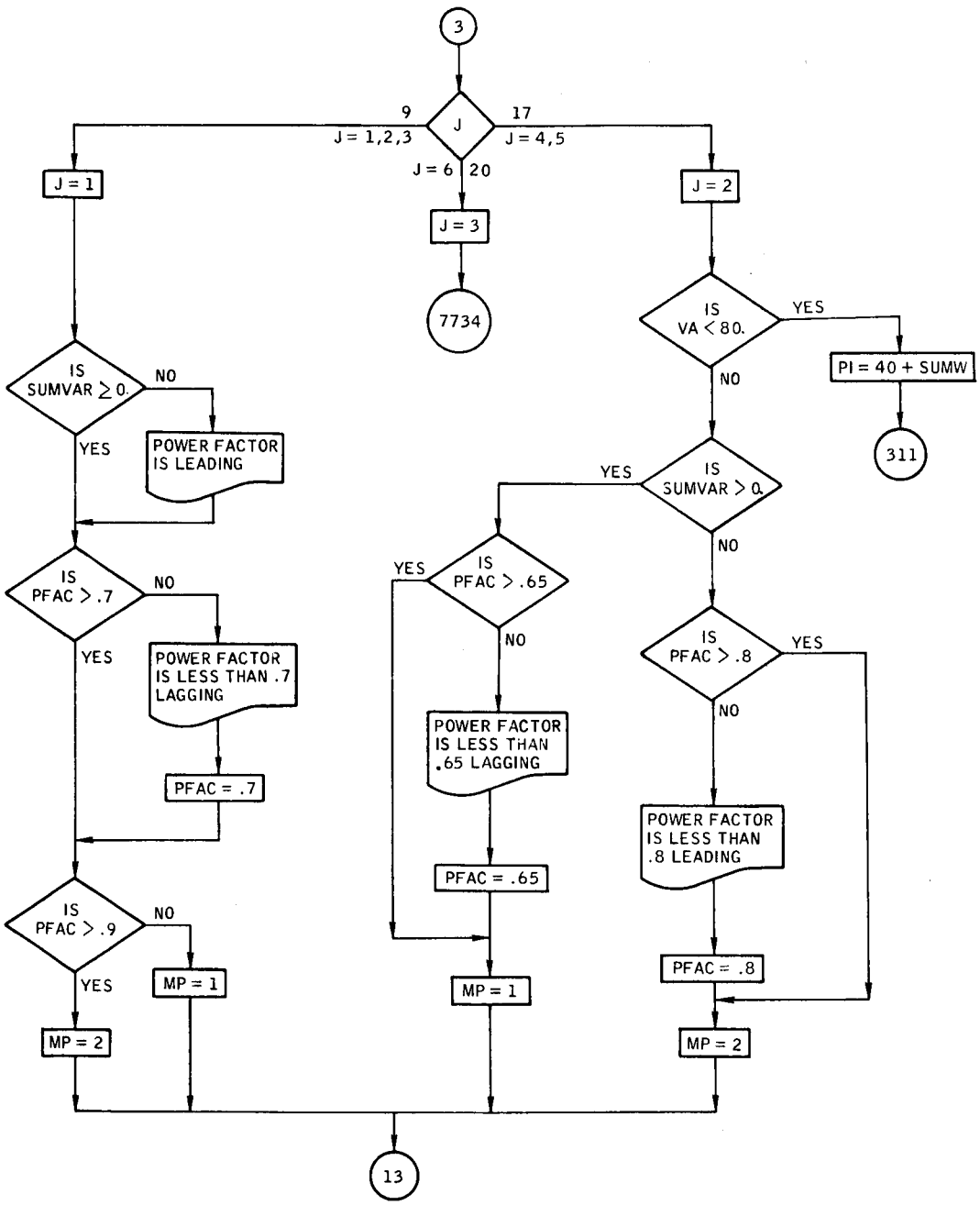
6.0 AAP INVERTER



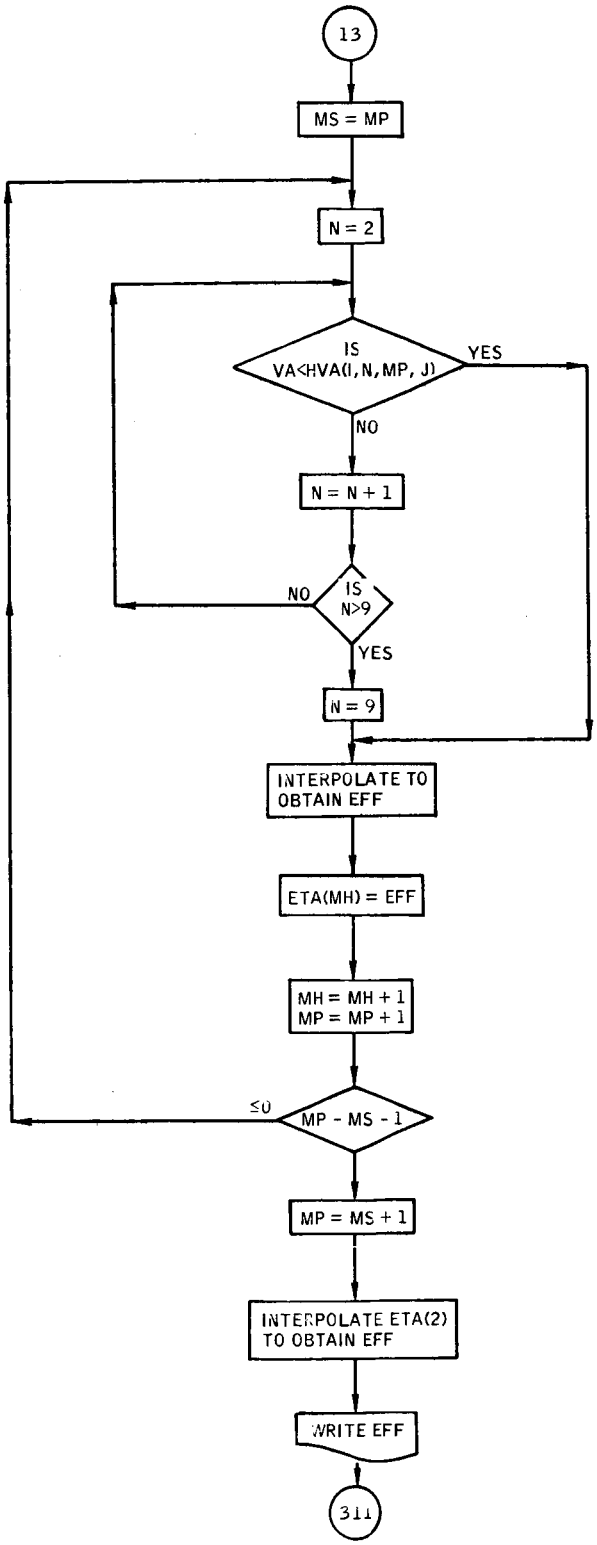
Flowchart 6-1.- AAP inverter.



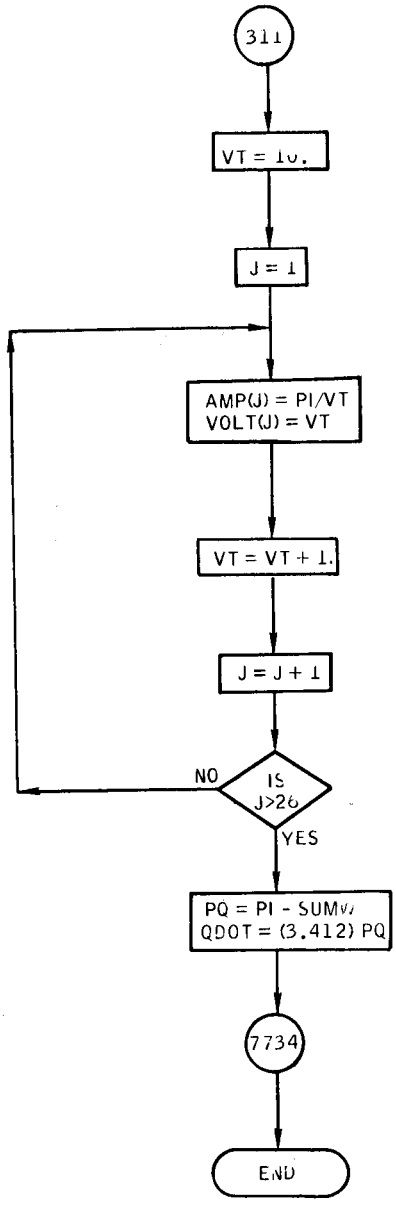
Flowchart 6-1.- Continued.



Flowchart 6-1.- Continued.



Flowchart 6-1.- Continued.



Flowchart 6-1.- Concluded.

7.0 PROGRAM LISTING

TABLE 7-I.- PROGRAM LISTING

```
00101    1*          DIMENSION ITEM(9),EQUIP(9),WATTS(9),PF(9),ACLOAD(9),INV(6),AK(6)
00103    2*          DATA EQUIP,WATTS,PF/6HSTEREO,6HTV     ,6HLAMP  ,6HRADIO ,6HHEATER,
00103    3*         16HMIXER ,6HCLOCK ,6HORDEAL,6H0-BALL, 50., 80.,200.,250.,300.,
00103    4*         2400.,500.,700.,900.,-.7,-.9,.8,1.,-.85,1.,.9,.6,1./
00107    5*          DIMENSION ETA(2),HVA(2,9,3,2),PFC(3,2),VOLT(26),AMP(26)
00110    6*          DATA HVA,PFC/300.,.615,.460,.666,.625,.698,.795,.721,1000.,.732,
00110    7*         21200.,.736,1400.,.734,1600.,.726,1900.,.702,300.,.662,470.,.712,
00110    8*         3690.,.746,900.,.762,1070.,.764,1290.,.76,1500.,.754,1635.,.747,
00110    9*         41810.,.73,250.,.7,520.,.78,700.,.756,800.,.767,910.,.77,1160.,.768

00110   10*          5,1500.,.75,1630.,.743,1900.,.72,68.,.5,81.,.575,112.,.642,160.,
00110   11*          6,697,210.,.733,280.,.754,345.,.758,426.,.754,500.,.743,75.,.652,
00110   12*          7108.,.71,140.,.742,185.,.772,240.,.785,280.,.79,368.,.786,430.,
00110   13*          8,781,500.,.768,75.,.6,90.,.635,125.,.688,175.,.728,225.,.748,290.,
00110   14*          9,76,360.,.768,428.,.765,500.,.755,.7,.9,1.,.65,1.,.8/
00113   15*           DATA AK/1250.,1250.,1250.,350.,350.,0./
00116   16*           DO 77 KID = 1,2
00120   17*           READ(5,1)LUMP,ITEM
00127   18*         1 FORMAT(2I1,8I2)
00130   19*           IF(LUMP.EQ.1)GO TO 201
00132   20*           L=0
00133   21*           SUMW = 0.
00134   22*           SUMVAR = 0.
00135   23*           DO 2 J=1,9
00140   24*           IF(ITEM(J).EQ.0)GO TO 2
00142   25*           SUMW = SUMW + WATTS(J)
00143   26*           VAR = WATTS(J)*SQRT((1./PF(J))**2-1.)
00144   27*           VAR = SIGN(VAR,PF(J))
00145   28*           SUMVAR = SUMVAR + VAR
00146   29*           L=L+1
00147   30*           ACLOAD(L) = EQUIP(J)
00150   31*         2 CONTINUE
00152   32*           VA = SQRT((SUMW**2) + (SUMVAR**2))
00153   33*           PFAC = SUMW/VA
00154   34*           READ(5,4)INV
00162   35*         4 FORMAT(6I2)
00163   36*           DO 5 J=1,6
00166   37*           IF(INV(J).EQ.1)GO TO 6
00170   38*         5 CONTINUE
00172   39*           GO TO 7734
00173   40*       201 READ(5,202)J,SUMW,POWF
00200   41*       202 FORMAT(I2,8X,2F10.4)
00201   42*           PFAC = ABS(POWF)
00202   43*           VA = SUMW/PFAC
00203   44*           SUMVAR = SQRT(VA**2 - SUMW**2)
00204   45*           SUMVAR = SIGN(SUMVAR,POWF)
00205   46*         6 WRITE(6,3)SUMW,SUMVAR,VA,PFAC
00213   47*         3 FORMAT(1H1,4HP = ,F10.3/5HQQ = ,F10.3/6HVA = ,F10.3/6HPF = ,F10.
00243   48*          23)
00244   49*           IF(VA.LE.AK(J))GO TO 8
00216   50*           WRITE(6,7)J,(ACLOAD(I),I=1,L)
00225   51*         7 FORMAT(15HO*****INVERTER ,I1,16H OVERLOADED*****/3X,8HAC LOADS/
00225   52*          2(1X,A6))
00226   53*     C
00225   54*     C      CALCULATION OF EFFICIENCY
00285   55*     C
```

TABLE 7-I.- PROGRAM LISTING - Continued

```
00236    56*        8 MH=1
00237    57*          GO TO(9,9,9,17,17,20),J
00230    58*        9 J=1
00231    59*          IF(SUMVAR.GE.0.)GO TO 92
00233    60*          WRITE(6,91)
00235    61*       91 FORMAT(24HOPOWER FACTOR IS LEADING)
00236    62*       92 IF(PFAC.GT.0.7)GO TO 11
00240    63*          WRITE(6,10)
00242    64*       10 FORMAT(1X,36HPOWER FACTOR IS LESS THAN .7 LAGGING)
00243    65*          PFAC = .7
00244    66*       11 IF(PFAC.GT.0.9)GO TO 12
00246    67*          MP=1
```

```
00247    68*          GO TO 13
00250    69*       12 MP=2
00251    70*       13 MS=MP
00252    71*      131 DO 14 N=2,9
00255    72*          IF(VA.LT.HVA(1,N,MP,J))GO TO 15
00257    73*       14 CONTINUE
00261    74*          N=9
00262    75*       15 EFF =(VA - HVA(1,N-1,MP,J))*(HVA(2,N,MP,J) - HVA(2,N-1,MP,J))/
00262    76*         2(HVA(1,N,MP,J) - HVA(1,N-1,MP,J)) + HVA(2,N-1,MP,J)
00263    77*          ETA(MH) = EFF
00264    78*          MH=MH+1
00265    79*          MP=MP+1
00266    80*          IF(MP-MS-1)131,131,16
00271    81*       16 MP = MS + 1
00272    82*          EFF = (PFAC - PFC(MS,J))*(ETA(2) - ETA(1))/   (PFC(MP,J) -PFC(MS,
00272    83*         2J)) + ETA(1)
00273    84*          GO TO 30
00274    85*       17 J=2
00275    86*          IF(VA.LT.80.)GO TO 66
00277    87*          IF(SUMVAR.GT.0.)GO TO 18
00301    88*          IF(PFAC.GT.0.8)GO TO 172
00303    89*          WRITE(6,171)
00305    90*      171 FORMAT(1X,36HPOWER FACTOR IS LESS THAN .8 LEADING)
00306    91*          PFAC = .8
00307    92*      172 MP=2
00310    93*          GO TO 13
00311    94*       66 PI = 40. + SUMW
00312    95*          GO TO 311
00313    96*       18 IF(PFAC.GT.0.65)GO TO 182
00315    97*          WRITE(6,181)
00317    98*      181 FORMAT(1X,37HPOWER FACTOR IS LESS THAN .65 LAGGING)
00320    99*          PFAC = .65
00321   100*      182 MB=1
00322   101*          GO TO 13
00323   102*       30 WRITE(6,31)EFF
00326   103*       31 FORMAT(7HOEFF = ,F10.7)
00327   104*          PI = SUMW/EFF
00330   105*      311 VT = 10.
00331   106*          DO 33 J=1,26
00334   107*          AMP(J) = PI/VT
00335   108*          VOLT(J) = VT
00336   109*       33 VT = VT + 1.
00340   110*          PQ = PI - SUMW
00341   111*          QDOT = 3.412 * PQ
```

TABLE 7-I.- PROGRAM LISTING - Concluded

```
00342   112*          WRITE(6,203)
00344   113*      203 FORMAT(1HQ,13X,8HPOWER IN,12X,10HPOWER LOST,11X,9HBTUS LOST)
00345   114*          WRITE(6,35)PI,PQ,QDOT
00352   115*       35 FORMAT(1X,3F20.3)
00353   116*          WRITE(6,204)
00355   117*      204 FORMAT(1HQ,12X,5HVOLTS,15X,4HAMPS)
00356   118*          WRITE(6,36)(VOLT(I),AMP(I),I = 1,26)
00365   119*       36 FORMAT(2F20.7)
00366   120*       20 J=3
00367   121*     7734 CONTINUE
00370   122*       77 CONTINUE
00372   123*          STOP
00373   124*          END
```

8.0 PROGRAM SAMPLE CASES

TABLE 8-I.- SAMPLE CASE 1

```
P =    1400.000

Q =   -2044.473

VA =    2477.876

PF =        .565

*****INVERTER 1 OVERLOADED*****
  AC LOADS
@@@@@@

POWER FACTOR IS LEADING
POWER FACTOR IS LESS THAN .7 LAGGING

EFF =    .6557699
```

POWER IN	POWER LOST	BTUS LOST
2134.895	734.895	2507.462

VOLTS	AMPS
10.0000000	213.4895077
11.0000000	194.0813694
12.0000000	177.9079227
13.0000000	164.2226982
14.0000000	152.4925041
15.0000000	142.3263378
16.0000000	133.4309425
17.0000000	125.5820627
18.0000000	118.6052818
19.0000000	112.3628988
20.0000000	106.7447538
21.0000000	101.6616697
22.0000000	97.0406847
23.0000000	92.8215246
24.0000000	88.9539614
25.0000000	85.3958025
26.0000000	82.1113491
27.0000000	79.0701876
28.0000000	76.2462521
29.0000000	73.6170712
30.0000000	71.1631689
31.0000000	68.8675823
32.0000000	66.7154713
33.0000000	64.6937895
34.0000000	62.7910314
35.0000000	60.9970021

TABLE 8-II.- SAMPLE CASE 2

P = 250.000

Q = .000

VA = 250.000

PF = 1.000

EFF = .7862500

POWER IN	POWER LOST	BTUS LOST
317.965	67.965	231.897

VOLTS	AMPS
10.0000000	31.7965021
11.0000000	28.9059110
12.0000000	26.4970851
13.0000000	24.4588478
14.0000000	22.7117872
15.0000000	21.1976681
16.0000000	19.8728139
17.0000000	18.7038248
18.0000000	17.6647234
19.0000000	16.7350011
20.0000000	15.8982511
21.0000000	15.1411915
22.0000000	14.4529555
23.0000000	13.8245661
24.0000000	13.2485425
25.0000000	12.7186009
26.0000000	12.2294239
27.0000000	11.7764822
28.0000000	11.3558936
29.0000000	10.9643111
30.0000000	10.5988340
31.0000000	10.2569362
32.0000000	9.9364070
33.0000000	9.6353036
34.0000000	9.3519124
35.0000000	9.0847149

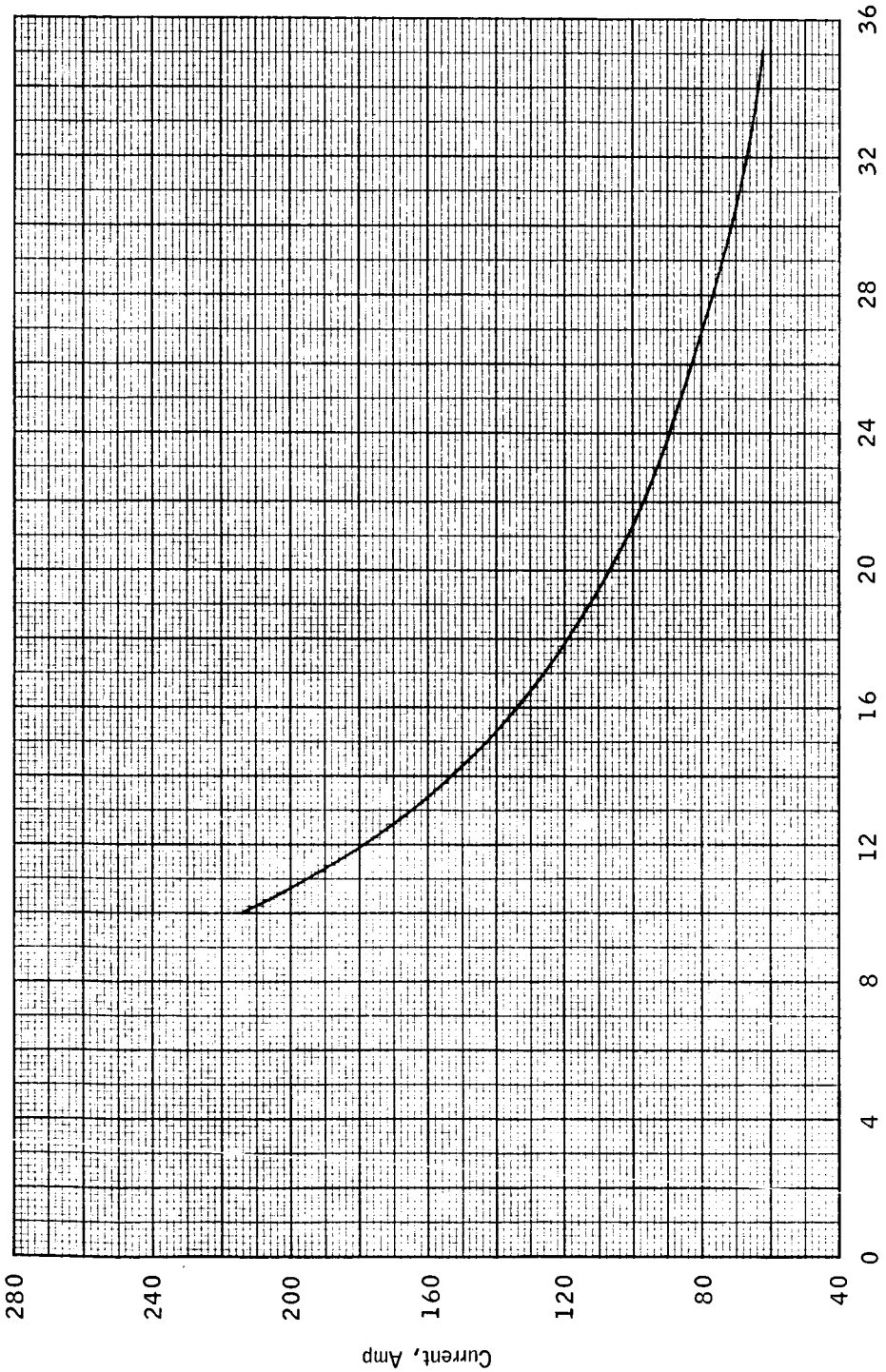


Figure 8-1.- Constant power curve samply case number 1, 1400 watts, .565 leading power factor.

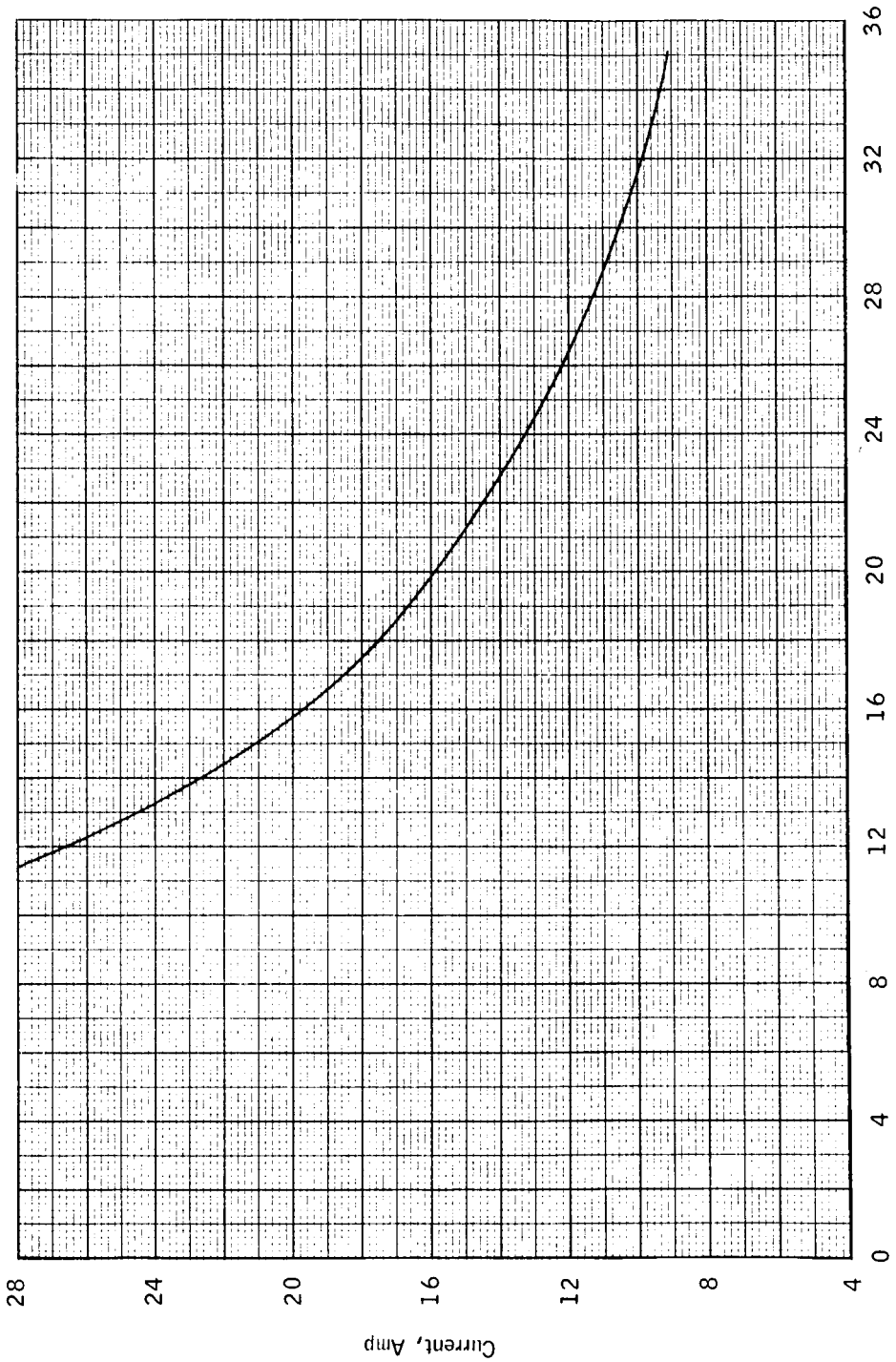


Figure 8-2.- Constant power curve sample case number 2, 250 watts unity power factor.

9.0 REFERENCES

1. Apollo Operations Handbook. SM2A-03-Block II Subsection 2.6 Electrical Power System. 1 March 1967.

2. Harold Dunham: Electrical Power Subsystem Study Guide-Lunar Module LM-3. LSG 770-430-43-LM-3, August 1968.

3. Spacecraft Operational Data Book SNA-8-D-027 (II) Rev 1, Environmental Control System. June 1968.